Front End Electronics for the STAR TPC

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The front end electronics (FEE) for the STAR TPC receives signals from the 136,600 pads on the TPC, amplifies them, shapes them, and digitizes them with a 512 time sample, 6/12 MHz, 10 bit waveform digitization system[1]. The high channel count requires a highly integrated design to minimize size, power, and costs, and to maximize reliability[2].

The analog functionality is contained in two custom 1.2 μ CMOS chips, the STAR Amplifier/Shaper (SAS), which contains a low noise preamplifier, shaper (with tail correction), and output buffer[3], and the SCA, which contains a 512 time bucket switched capacitor array, plus a 12 bit ADC. Both chips are 16 channels wide, with 32 channels (2 chip sets) packaged onto 2.9" by 7" FEE cards. The FEE cards contain all of the analog circuitry, and plug onto the TPC sectors, eliminating cabling and associated ground loops. A water cooled aluminum bar maintains FEE temperature within 0.5 ^{o} C, necessary for accurate dE/dx measurement in the TPC.

The FEE cards are read out by readout boards, which control 36 FEE cards (1152 channels) of FEE. Data is sent from the readout boards to STAR DAQ over a fiber optic link at 1.2 Gbit/sec. A trigger bus provides trigger, abort and calibration event functionality, while a slow controls link provides for monitoring and control, such as turning groups of FEE cards on and off. The readout board sequencer, readout buffers, and control are implemented in FPGA's; the system can read out events at 200 Hz.

20 FEE cards and a prototype readout board are now in use in the STAR system test[4]. These tests have shown that the system meets it's requirements, and that the on-detector noise levels match the bench levels. Output stability with temperature, humidity and time have all been monitored, and grounding and cooling addressed.

The FEE cards went into low rate production (4% build, or 240 cards) at the end of 1996; full production is slated to begin in 1997, to be complete at STAR turn on in 1999. Readout board prototyping is almost complete, and production should follow a similar schedule.

Roughly 25,000 channels of this electronics will also be used for the STAR forward TPC's. This application takes advantage of the flexibility of the design; the SAS shaping time is adjusted to 400 nsec FWHM, and the SCA sampling clock and number of samples are reduced. Because of the reduced noise and output slew rate, SAS power consumption can be reduced to about 1/3 of that in the main TPC. The chips and circuitry will be repackaged to fit the allowable space. STAR will also provide 3840 channels of this electronics (plus spares) to the BRAHMS collaboration at RHIC, for use with their TPC's.

References

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[3] E. Beuville *et al.*, "A Low Noise Amplifier-Shaper with Tail Correction for the STAR Detector", IEEE Transactions on Nuclear Science **43**, 1619 (1996).

[4] W. Betts *et al.*, Results from the STAR TPC System Test. , preprint CU (Creighton U.) -PHY-NP 96/03, Nov. 1996, submitted to IEEE Transactions on Nuclear Science.